

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims:

- 1           1. (Currently amended) A method for latching and amplifying a  
2   capacitively coupled inter-chip communication signal, comprising:  
3           receiving an input signal on a capacitive receiver pad from a capacitive  
4   transmitter pad;  
5           feeding the input signal through an inverter to produce an output signal;  
6           feeding the output signal through a weakened inverter to produce a  
7   feedback signal;  
8           feeding the feedback signal back into an input of the inverter so as to form  
9   a latch for the input signal between the inverter and the weakened inverter; and  
10          establishing a high bias voltage,  $V_H$ , with a high bias voltage generator and  
11          establishing a low bias voltage,  $V_L$ , with a low bias voltage generator;  
12          wherein the high bias voltage generator includes a mechanism for  
13          adjusting the high bias voltage,  $V_H$ ;  
14          wherein the low bias voltage generator includes a mechanism for adjusting  
15          the low bias voltage,  $V_L$ ;  
16          wherein the weakened inverter is biased to produce the feedback signal  
17   that swings between a the high bias voltage,  $V_H$ , and a the low bias voltage,  $V_L$ ;  
18   and  
19          ~~adjusting an RC time constant for the feedback signal so that the time~~  
20   ~~constant for the feedback signal is significantly larger than the time constant for~~

21 | ~~the transmitted signal from the capacitive transmitter pad, thereby ensuring that~~  
22 | ~~the feedback signal does not mask transitions of the transmitted signal;~~  
23 |       wherein  $V_H$  is slightly higher than a switching threshold of the inverter, and  
24 |  $V_L$  is slightly lower than the switching threshold of the inverter, whereby the  
25 | feedback signal causes the input signal to reside within a narrow voltage range  
26 | near the switching threshold of the inverter, thereby making the inverter sensitive  
27 | to small transitions in the input signal received on the capacitive receiver pad.

1       2. (Original) The method of claim 1, further comprising amplifying an  
2       output of the inverter through an amplification stage to produce an amplified  
3       output signal.

1       3-4 (Canceled).

1 |       5. (Currently amended) The method of ~~claim 4~~claim 2, further comprising  
2 |       adjusting the high bias voltage generator and the low bias voltage generator to  
3 |       provide a specified sensitivity to transitions of the input signal.

1 |       6. (Currently amended) The method of ~~claim 4~~claim 2, further comprising  
2 |       adjusting the high bias voltage generator and the low bias voltage generator to  
3 |       provide a specified noise immunity to noise associated with the input signal.

1       7 (Canceled).

1       8. (Currently amended) An apparatus for latching and amplifying a  
2       capacitively coupled inter-chip communication signal, comprising:  
3       a receiving mechanism configured to receive an input signal on a  
4       capacitive receiver pad from a capacitive transmitter pad;

5 a latching mechanism configured to feed the input signal through an  
6 inverter to produce an output signal; and  
7 a biasing mechanism configured to establishing a high bias voltage,  $V_H$ ,  
8 with a high bias voltage generator and establishing a low bias voltage,  $V_L$ , with a  
9 low bias voltage generator;  
10 wherein the high bias voltage generator includes a mechanism for  
11 adjusting the high bias voltage,  $V_H$ ;  
12 wherein the low bias voltage generator includes a mechanism for the low  
13 bias voltage,  $V_L$ ;  
14 ~~an adjusting mechanism configured to adjust an  $RC$  time constant for the~~  
15 ~~feedback signal so that the time constant for the feedback signal is significantly~~  
16 ~~larger than the time constant for the transmitted signal from the capacitive~~  
17 ~~transmitter pad, thereby ensuring that the feedback signal does not mask~~  
18 ~~transitions of the transmitted signal;~~  
19 wherein the latching mechanism is further configured to feed the output  
20 signal through a weakened inverter to produce a feedback signal; and  
21 wherein the latching mechanism is further configured to feed the feedback  
22 signal back into an input of the inverter so as to form a latch for the input signal  
23 between the inverter and the weakened inverter;  
24 wherein the weakened inverter is biased to produce the feedback signal  
25 that swings between ~~a~~the high bias voltage,  $V_H$ , and ~~a~~the low bias voltage,  $V_L$ ;  
26 and  
27 wherein  $V_H$  is slightly higher than a switching threshold of the inverter, and  
28  $V_L$  is slightly lower than the switching threshold of the inverter, whereby the  
29 feedback signal causes the input signal to reside within a narrow voltage range  
30 near the switching threshold of the inverter, thereby making the inverter sensitive  
31 to small transitions in the input signal received on the capacitive receiver pad.

1           9. (Original) The apparatus of claim 8, further comprising an amplifying  
2 mechanism configured to amplify an output of the inverter through an  
3 amplification stage to produce an amplified output signal.

1           10-11 (Canceled).

1           12. (Currently amended) The apparatus of ~~claim 11~~claim 9, further  
2 comprising an adjusting mechanism configured to adjust the high bias voltage  
3 generator and the low bias voltage generator to provide a specified sensitivity to  
4 transitions of the input signal.

1           13. (Currently amended) The apparatus of ~~claim 11~~claim 9, further  
2 comprising an adjusting mechanism configured to adjust the high bias voltage  
3 generator and the low bias voltage generator to provide a specified noise  
4 immunity to noise associated with the input signal.

1           14 (Canceled).

1           15. (Currently amended) A means for latching and amplifying a  
2 capacitively coupled inter-chip communication signal, comprising:  
3           a receiving means for receiving an input signal on a capacitive receiver  
4 pad from a capacitive transmitter pad;  
5           a latching means configured to feed the input signal through an inverter to  
6 produce an output signal; and  
7           a biasing means for establishing a high bias voltage,  $V_{H_2}$ , with a high bias  
8 voltage generator and for establishing a low bias voltage,  $V_{L_2}$ , with a low bias  
9 voltage generator;

10        wherein the high bias voltage generator includes a mechanism for  
11        adjusting the high bias voltage,  $V_H$ ; and  
12        wherein the low bias voltage generator includes a mechanism for the low  
13        bias voltage,  $V_L$ ;  
14        ~~an adjusting means for adjusting an  $RC$  time constant for the feedback~~  
15        ~~signal so that the time constant for the feedback signal is significantly larger than~~  
16        ~~the time constant for the transmitted signal from the capacitive transmitter pad,~~  
17        ~~thereby ensuring that the feedback signal does not mask transitions of the~~  
18        ~~transmitted signal;~~  
19        wherein the latching means is further configured to feed the output signal  
20        through a weakened inverter to produce a feedback signal; and  
21        wherein the latching means is further configured to feed the feedback  
22        signal back into an input of the inverter so as to form a latch for the input signal  
23        between the inverter and the weakened inverter;  
24        wherein the weakened inverter is biased to produce the feedback signal  
25        that swings between a the high bias voltage,  $V_H$ , and a the low bias voltage,  $V_L$ ;  
26        and  
27        wherein  $V_H$  is slightly higher than a switching threshold of the inverter, and  
28         $V_L$  is slightly lower than the switching threshold of the inverter, whereby the  
29        feedback signal causes the input signal to reside within a narrow voltage range  
30        near the switching threshold of the inverter, thereby making the inverter sensitive  
31        to small transitions in the input signal received on the capacitive receiver pad.

1        16. (Original) The means of claim 15, further comprising an amplifying  
2        means for amplifying an output of the inverter through an amplification stage to  
3        produce an amplified output signal.

1        17-18 (Canceled).

1 | 19. (Currently amended) The means of ~~claim 18~~claim 16, further  
2 | comprising an adjusting means for adjusting the high bias voltage generator and  
3 | the low bias voltage generator to provide a specified sensitivity to transitions of  
4 | the input signal.

1 | 20. (Currently amended) The means of ~~claim 18~~claim 16, further  
2 | comprising an adjusting means for adjusting the high bias voltage generator and  
3 | the low bias voltage generator to provide a specified noise immunity to noise  
4 | associated with the input signal.

1 | 21 (Canceled).

1 | 22. (New) The method of claim 1, further comprising adjusting an *RC* time  
2 | constant for the feedback signal so that the time constant for the feedback signal is  
3 | significantly larger than the time constant for the transmitted signal from the  
4 | capacitive transmitter pad, thereby ensuring that the feedback signal does not  
5 | mask transitions of the transmitted signal.

1 | 23. (New) The apparatus of claim 8, further comprising an adjusting  
2 | mechanism configured to adjust an *RC* time constant for the feedback signal so  
3 | that the time constant for the feedback signal is significantly larger than the time  
4 | constant for the transmitted signal from the capacitive transmitter pad, thereby  
5 | ensuring that the feedback signal does not mask transitions of the transmitted  
6 | signal.

1 | 24. (New) The means of claim 15, further comprising an adjusting means  
2 | for adjusting an *RC* time constant for the feedback signal so that the time constant  
3 | for the feedback signal is significantly larger than the time constant for the

- 4 transmitted signal from the capacitive transmitter pad, thereby ensuring that the
- 5 feedback signal does not mask transitions of the transmitted signal.